Application No. 10/680,884
Amndt.dated: June 15, 2006
Reply to Office Action mailed: June 07, 2006

Amendments to the Specification:

Please replace paragraph **[0017]** with the following rewritten paragraph:

- -**[0017]** The synchronization and error detection/correction modulel24 provides an interface between the megacell 122 and the bus 110. In general, the module 124 synchronizes source synchronous data received via the bus 110 to a clock signal generated and/or used internally to the bus devices 108, 112, 114, 116. Thus, the synchronization and error detection/correction module ~~[[1240]]~~ 124 provides synchronized data to the megacell 122. To comply with the applicable bus protocol (e.g., PCI-X 2.0), a finite amount of time is allocated for the synchronization and error detection/correction module to synchronize the data. The synchronization and error detection/correction module 124 also may receive common clock data which does not require synchronization.- -

Please replace paragraph **[0026]** with the following rewritten paragraph:

- -**[0026]** For source synchronous data transactions and as mentioned above, a finite amount of time is allocated for the synchronization process to occur per the applicable protocol implemented on bus 110. In accordance with exemplary embodiments of the invention, for source synchronous data transactions, the ECC-based error detection and correction (to the extent correctable errors have occurred) occurs during the time period allocated for synchronization. As such, error detection and correction occurs "concurrently" with the data synchronization. In this context and as used in the claims, concurrent does not require the error detection/correction and data synchronization processes to occur simultaneously. Concurrent means that in the time allocated for synchronization, both synchronization and error detection and correction occur. In some embodiments, however, both synchronization and error detection and correction may occur simultaneously. Because ECC error detection and correction occurs concurrently with the data reception and synchronization function performed by the data synchronizing logic 150, latency is reduced relative to what would have been the case if the error detection and correction function occurred after the complete reception and synchronization of all data from bus 110. Thus, by incorporating error detection and correction logic into the synchronization and error detection/correction module 124, overall performance is improved compared to what would likely be the case if error detection and correction were the sole responsibility of the megacell 122. Performing error detection and correction concurrently with synchronization is facilitated by the ~~[[PC-X 2.0]]~~ PCI-X 2.0 protocol, to the extent this protocol is implemented on bus 110, because per the PCI-X 2.0 protocol, ECC bits are transmitted with the associated data and address bits.- -

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